NOT RECOMMENDED FOR NEW DESIGNS
POSSIBLE SUBSTITUTE
PRODUCT: ISL6412

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Author: Manisha Pandya

Introduction

The ISL6414 integrates three ultra low noise, low dropout linear regulators providing a highly integrated single-chip solution for 802.11 wireless chipset architectures. It operates from 3.0V to 3.8V input and provides preset output voltages - LDO1 set at 1.8V, LDO2 and LDO3 set at 2.84V.

The device features power sequencing specifically for wireless chipsets. The outputs are sequenced such that LDO1, the 1.8V core regulator voltage, is always within regulation before LDO2, the 2.84V output LDO, is sequenced on. When powering down, power to the 2.84V LDO2 is removed before the 1.8V LDO1 core regulator is sequenced off.

Designed with an internal P-channel MOSFET pass transistor, the ISL6414 operates with a low supply current. An output fault detection circuit indicates loss of regulation on any of the three outputs. Other features include a logic controlled shutdown mode, short circuit and thermal shutdown protection, and reverse battery protection.

The ISL6414 also includes a RESET function. Integration of this function into the ISL6414 eliminates the additional RESET IC and external support components required in wireless chipset power supply applications. The IC asserts a RESET signal whenever the V_{CC} (IN) supply voltage drops below a preset threshold, keeping it asserted for at least 100ms after V_{CC} (IN) has risen above the reset threshold. Two RESET outputs are provided; $\overline{\text{RESET}}$ is a push-pull active-LOW output, while RESET is an active-HIGH output.

Applications

- PRISM® 3, PRISM GT™, and PRISM WWR Chipsets
- WLAN Cards
  - PCMCIA, Cardbus32, MiniPCI Cards
  - Compact Flash Cards
- Hand-Held Instruments

ISL6414 Reference Design

TABLE 1. ISL6414 EVALUATION BOARD

BOARD NAME	IC PART NUMBER	PACKAGE
ISL6414EVAL1	ISL6414IR	16-Ld QFN

Quick Start Evaluation

The evaluation board is shipped “ready to use” right from the box. The board accepts a 3.3V input from a standard power supply. The output can be exercised through the use of an external load.

There are posts available on the board for introducing power to the board and for drawing current from the regulated outputs. Post connectors are also available to monitor power good conditions FAULT (P11), RESET (P9) and $\overline{\text{RESET}}$ (P10). Posts for Shutdown functions SHDN (P12) and SHDN3 (P13) allows low power mode function testing.

Each evaluation board kit is sent with 5 samples of ISL6414IR.

Recommended Test Equipment

To test the functionality of the ISL6414, the following equipment is recommended:

- An adjustable 0V - 5V, 2A capable bench power supply
- An electronic load
- A Four channel oscilloscope with probes
- A Precision digital multimeter

Power and Load Connections

Input Voltage - Connect the positive lead of the adjustable bench power supply to the 3.3V post (P3). Connect the ground lead of the supply to GND post (P4).

Output Voltages - The ISL6414EVAL1 provides fixed output voltages for use in Wireless Chipset applications. Internal trimmed resistor networks inside the chip set the nominal output voltages as below:

V_{OUT1} = 1.8V (P5)

V_{OUT2} = 2.84V (P7)

V_{OUT3} = 2.84V (P1)

The outputs can be exercised through external load on connectors. The maximum currents are V_{OUT1} - 500mA, V_{OUT2} - 300mA and V_{OUT3} -200mA.

Output Loading, Sourcing Current - To load the V_{OUT1} output connect the positive lead of the electronic load to the V_{OUT1} (P5) post and the return terminal of the same load channel to the GND (P6) post. Similarly connect the positive terminal of the second load channel to the V_{OUT2} (P7) post and the return terminal to the GND (P8) post to load the output of LDO2. The LDO3 output can be loaded by connecting the positive terminal of a third channel of the electronic load to the V_{OUT3} (P1) post and the return terminal to the GND (P2) post.

Evaluation Board Performance

ISL6414EVAL1 Evaluation board provides easy platform to characterize performance of the IC.

Output Performance

Figures below show transient response and regulation for LDO1, LDO2 and LDO3.

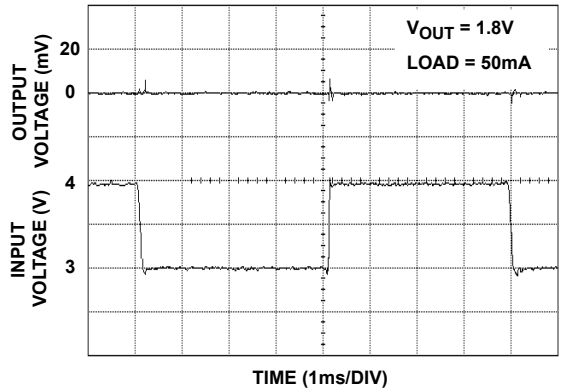


FIGURE 1. LINE TRANSIENT RESPONSE (V_{OUT1})

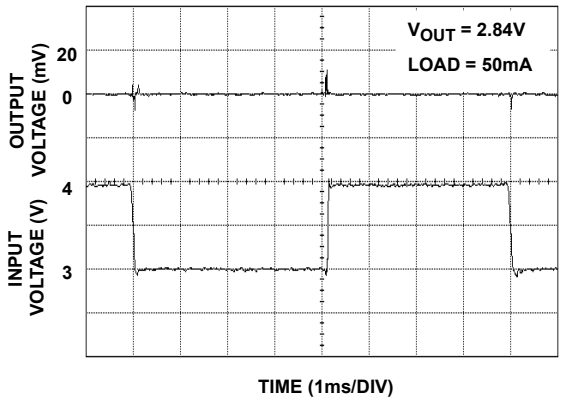


FIGURE 2. LINE TRANSIENT RESPONSE (V_{OUT2})

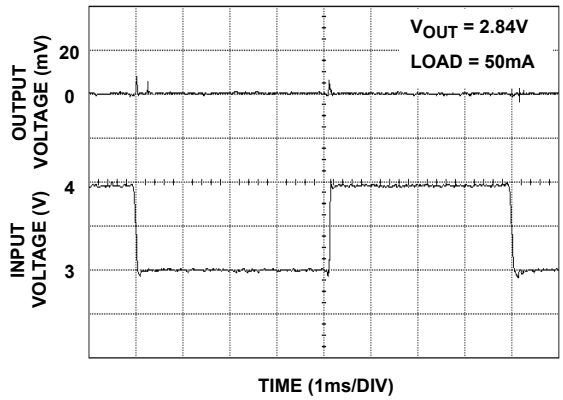


FIGURE 3. LINE TRANSIENT RESPONSE (V_{OUT3})

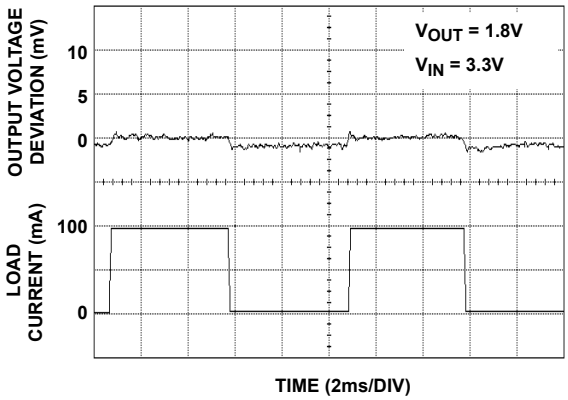


FIGURE 4. LOAD TRANSIENT RESPONSE (V_{OUT1})

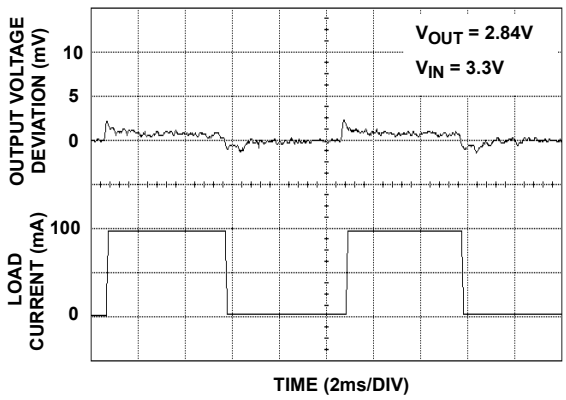


FIGURE 5. LOAD TRANSIENT RESPONSE (V_{OUT2})

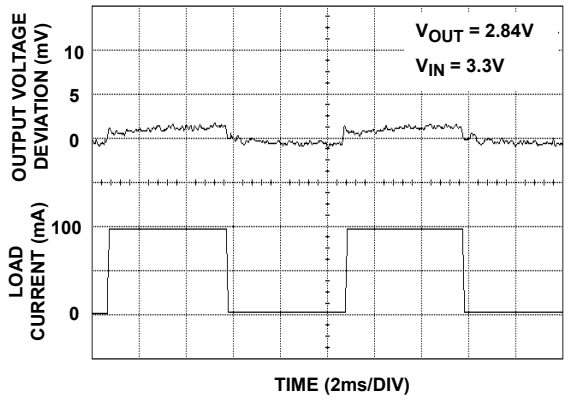


FIGURE 6. LOAD TRANSIENT RESPONSE (V_{OUT3})

Dropout Voltage

The ISL6414 features a typical 0.5Ω $r_{DS(ON)}$ P-channel MOSFET pass transistors. This provides several advantages over similar designs using PNP bipolar pass transistors. The P-Channel MOSFET requires no base drive, which reduces quiescent current considerably. PNP based regulators waste considerable current in dropout when the pass transistor saturates. They also use high base drive currents under large loads. The ISL6414 does not suffer from these problems and ultra low drop-out regulators to maintain 2.84V supplies within regulation with worst case minimum line input. Both LDO2 and LDO3 can supply full load with less then 3.0V input. Figure below shows the dropout voltage vs output load current for both LDO2 and LDO3.

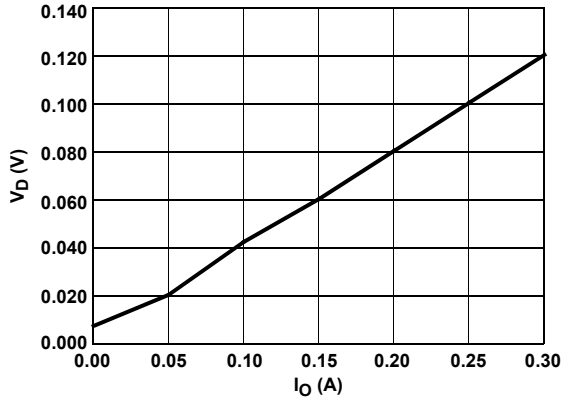


FIGURE 7. LD02 DROPOUT VOLTAGE

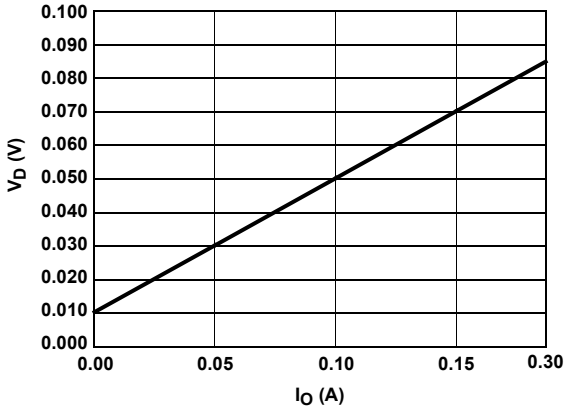


FIGURE 8. LD03 DROPOUT VOLTAGE

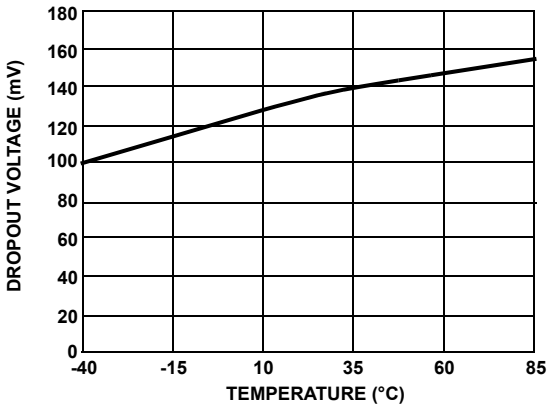


FIGURE 9. LD02 DROPOUT VOLTAGE vs TEMPERATURE

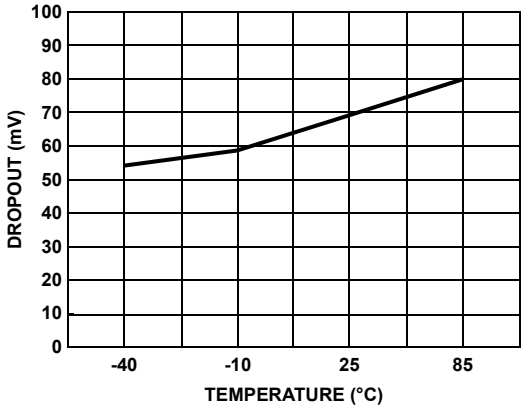


FIGURE 10. LD03 DROPOUT VOLTAGE vs TEMPERATURE

Current Limit

The ISL6414 monitors and controls the pass transistor's gate voltage to limit the output current. The current limit for LDO1 is 550mA, LDO2 is 330mA and LDO3 is 250mA. Performance in over current event can be tested by applying over load on respective LDO outputs. The FAULT output will go low for over current condition on any of the three LDO. The ISL6414 based DC-DC converter is fully protected from short circuit to ground outputs due to the current limit and thermal protection features.

Integrated RESET for MAC/ Baseband Processors

The ISL6414 includes a microprocessor supervisory circuit. This circuit eliminates the extra RESET IC and external components needed in wireless chipset applications. This block performs a single function; it asserts a RESET signal whenever the V_{IN} supply voltage decreases below a preset threshold 2.63V, keeping it asserted for a programmable time (set by external capacitor CT) after the V_{IN} pin voltage has risen above the RESET threshold.

The push pull output stage of the reset circuit provides both an active-Low $\overline{\text{RESET}}$ (P10) and an active-HIGH RESET (P9) output. This function is guaranteed to be in the correct state for V_{IN} down to 1V. In addition to issuing a reset to the microprocessor during power-up, power down and brownout conditions, this block is relatively immune to short duration, negative-going V_{IN} transients/glitches. Figure below shows the relations between RESET timing capacitor and programmable RESET delay.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the ISL6414. When the junction temperature (T_J) exceeds +150°C, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistor and allowing the IC to cool. The pass transistor turns on again after the IC's junction temperature cools 20°C, resulting in a pulsed output during continuous thermal overload conditions. Thermal overload protection protects the ISL6414 against fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of +150°C.

Shutdown

Driving the SHDN input (P12) LOW puts both LDO1 and LDO2 into shutdown mode. Driving the SHDN3 (P13) input LOW puts LDO3 in shutdown mode. Pulling the SHDN and SHDN3 pins LOW simultaneously, puts the entire chip into shutdown mode, and supply current drops to 5µA typical. External pull up resistors are not required because both SHDN and SHDN3 inputs have internal pull-up resistors, so that in normal operation the outputs are always enabled. During shutdown mode using the SHDN pin, the FAULT output will remain HIGH (refer to Figure 11).

Fault-Detection Circuitry

The FAULT pin monitors LDO1 output regulation, as well as fault conditions such as current limit and thermal shutdown. The FAULT output goes LOW, if the LDO1 output is out of regulation by ±5.5% (typ.). During shutdown mode using the SHDN pin, the FAULT output will remain HIGH (refer to Figure 11).

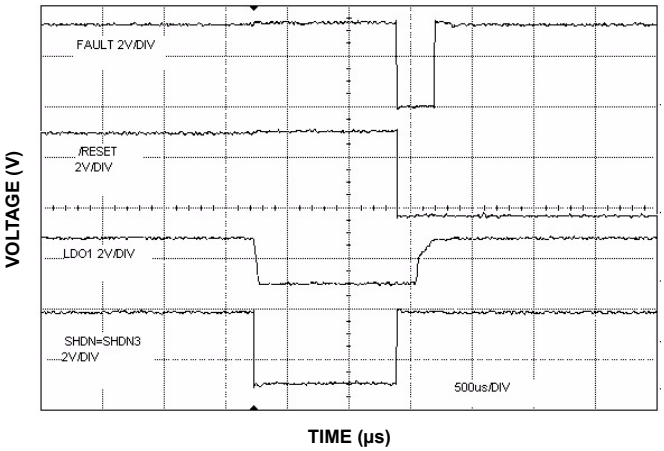


FIGURE 11. SHUTDOWN vs RESET and FAULT

Operating Region and Power Dissipation

The maximum power dissipation of ISL6414 depends on the thermal resistance of the IC package and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipated in the device is:

PT = P1 + P2 + P3, where

$P1 = I_{OUT1} (V_{IN} – V_{OUT1})$

$P2 = I_{OUT2} (V_{IN} – V_{OUT2})$

$P3 = I_{OUT3} (V_{IN}- V_{OUT3})$

The maximum allowed power dissipation is:

$P_{MAX} = (T_{JMAX} – T_A)/\theta_{JA}$

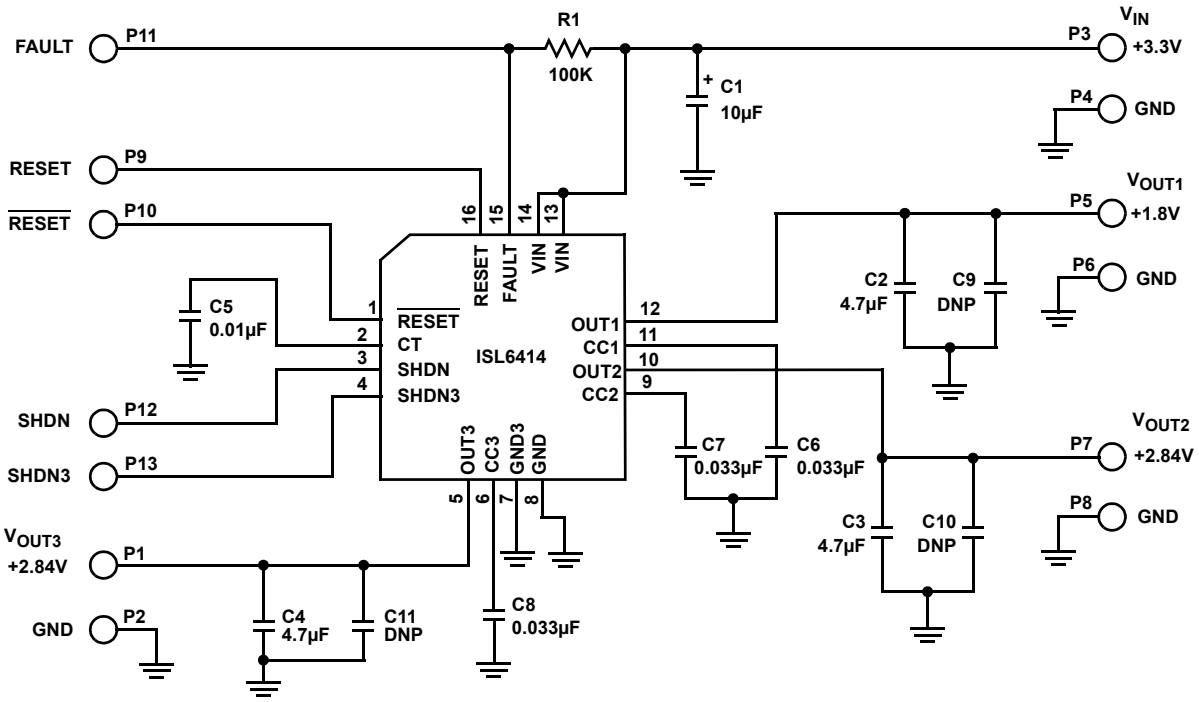
Where T_{JMAX} = 150°C, T_A = ambient temperature, and θ_{JA} is the thermal resistance from the junction to the surrounding environment.

References

For Intersil documents available on the web, see http://www.intersil.com/

[1] *ISL6414 Data Sheet,* Intersil Corporation, File No. FN9128.

ISL6414EVAL1 Schematic



ISL6414EVAL1 Bill of Materials

ITEM	REFERENCE	QTY	PART NUMBER	PART TYPE	DESCRIPTION	PACKAGE	VENDOR
1	U1	1	ISL6414IR	IC, Linear, Multi-Output	Regulator, Low Drop Out	16-Lead QFN 4x4	Intersil
CAPACITORS							
2	C1	1	1210ZC106MAT2A	Capacitor, Ceramic, X7R	10µF, 20%, 10V	SM_1210	AVX/Panasonic
3	C2, C3, C4	3	1210ZC475MAT2A	Capacitor, Ceramic, X7R	4.7µF, 20%, 10V	SM_1210	AVX/Panasonic
4	C9, C10, C11 (DNP)	3		Capacitor, Ceramic, X7R		SM_1210	AVX/Panasonic
5	C5	1	0603ZC103KAT2A	Capacitor, Ceramic, X7R	0.01µF, 10%, 10V	SM_0603	AVX/Panasonic
6	C6, C7, C8	3	0603ZC333JAT2A	Capacitor, Ceramic, X7R	0.033µF, 5%, 10V	SM_0603	AVX/Panasonic
RESISTORS							
7	R1	1		Resistor, Film	100kΩ, 5%, 0.1W	SM_0603	Panasonic
OTHERS							
8	P1 - P13	13	1514-2	Turrett Post	Terminal post, through-hole, 1/4 inch tall	PTH	Keystone

ISL6414EVAL1 Evaluation Board Layout

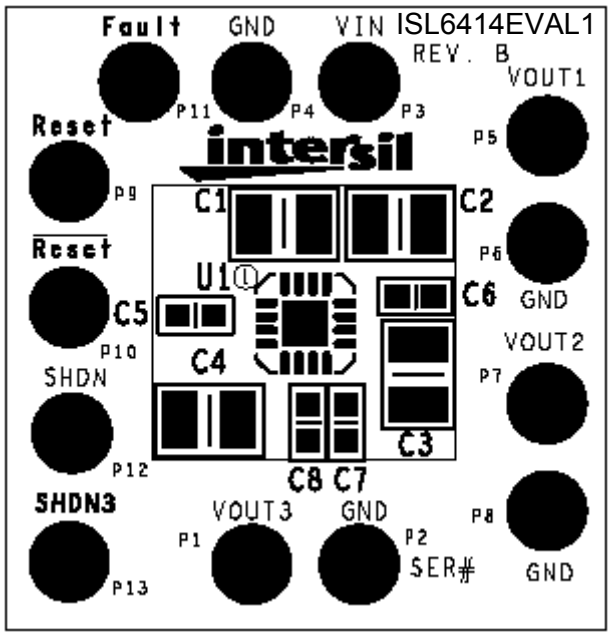


FIGURE 12. ISL6414EVAL1 - TOP LAYER SILK SCREEN

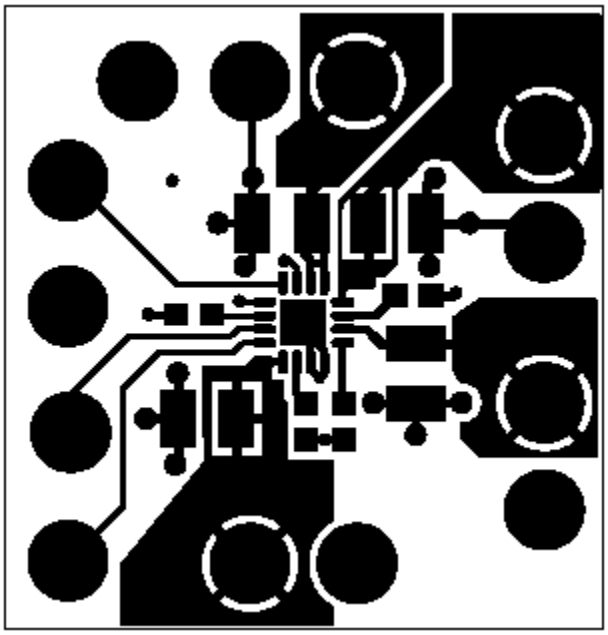


FIGURE 13. ISL6414EVAL1 - TOP LAYER

ISL6414EVAL1 Evaluation Board Layout (Continued)

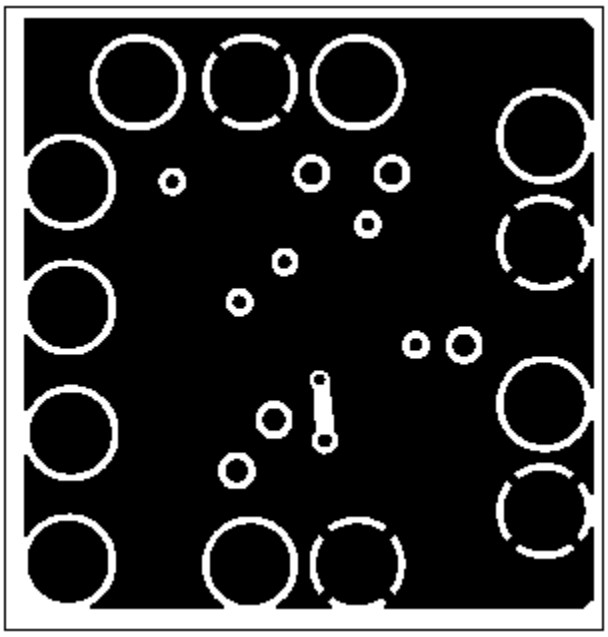


FIGURE 14. ISL6414EVAL1 - LAYER 2 (GROUND)

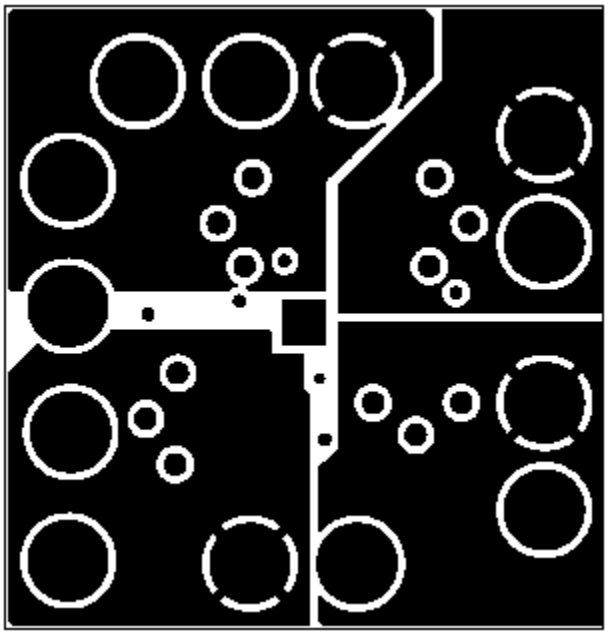


FIGURE 15. ISL6414EVAL1 - LAYER 3 (POWER)

ISL6414EVAL1 Evaluation Board Layout (Continued)

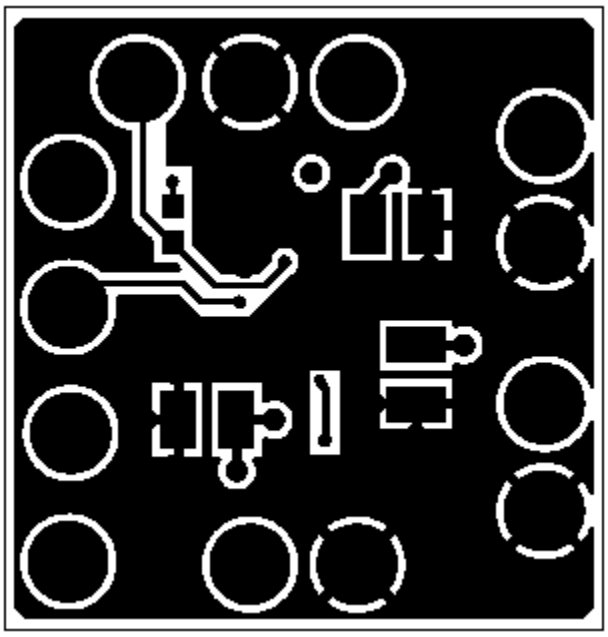


FIGURE 16. ISL6414EVAL1 - LAYER 4 (BOTTOM)

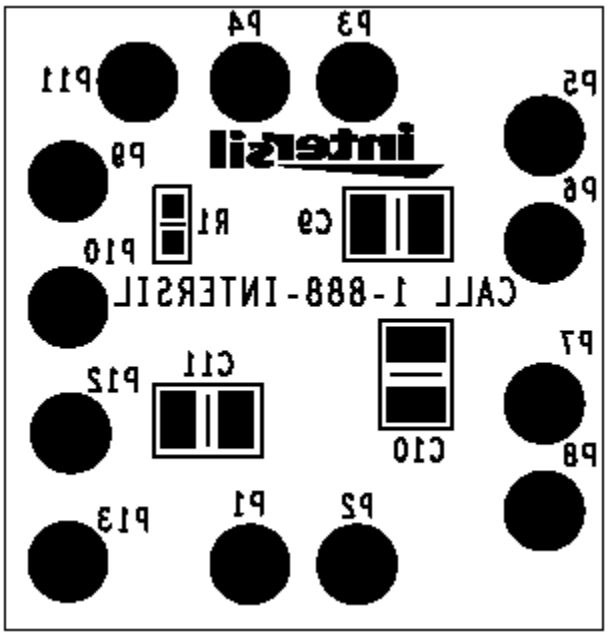


FIGURE 17. ISL6414EVAL1 - BOTTOM LAYER SILK SCREEN